

**This Page Is Inserted by IFW Operations
and is not a part of the Official Record**

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- **BLACK BORDERS**
- **TEXT CUT OFF AT TOP, BOTTOM OR SIDES**
- **FADED TEXT**
- **ILLEGIBLE TEXT**
- **SKEWED/SLANTED IMAGES**
- **COLORED PHOTOS**
- **BLACK OR VERY BLACK AND WHITE DARK PHOTOS**
- **GRAY SCALE DOCUMENTS**

IMAGES ARE BEST AVAILABLE COPY.

**As rescanning documents *will not* correct images,
please do not report the images to the
Image Problem Mailbox.**



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/371,955	08/11/1999	SHANE P. LEIPHART	M4065.0196/P	9847

24998 7590 01/17/2003

DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L STREET NW
WASHINGTON, DC 20037-1526

EXAMINER

KANG, DONGHEE

ART UNIT	PAPER NUMBER
----------	--------------

2811

DATE MAILED: 01/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/371,955

Applicant(s)

LEIPHART, SHANE P.

Examiner

Donghee Kang

Art Unit

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 November 2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 26-40 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 26, 27 and 38 is/are allowed.
- 6) ☒ Claim(s) 36 is/are rejected.
- 7) ☒ Claim(s) 28-35, 37 and 39-40 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 1 November 2002 has been entered.

Specification

2. The disclosure is objected to because of the following informalities:

The unit "Δ" is used for thickness of metal layer, for example 300 Δ titanium layer (see lines 8 & 32 on page 9 and lines 3 & 14 on page 10):

The unit Δ for thickness is not acceptable in the art. This should be change to "one of nm, μm and Å".

The unit "EC" is used for temperature, for example 465EC (see line 31 on page 9 & line 19 on page 10). The unit "EC" is not acceptable for temperature. This should be changed to "°C".

Appropriate correction is required.

Claim Objections

3. Claims **28, 33-37 & 39-40** are objected to because of the following informalities:

Referring to claim **28**, line 5: the phrase "the substrate" should be "the semiconductor substrate".

Referring to claims **33, 34 & 35**, line 6, respectively: the phrase "a substrate" should be "the semiconductor substrate" or "the substrate". The examiner suggests "the semiconductor substrate".

Referring to claim **36**, line 6: the phrase "a semiconductor substrate" should be "the semiconductor substrate".

Referring to claims **28, 35, 36, 37, 39 & 40**, lines 17, 16, 18, 12, 15 & 18, respectively: the phrase "the plug material" should be "the conductive plug material".

Referring to claim **40**, line 7 & 9, respectively: the phrase "said metallic layer" should be "said first metallic layer" and the phrase "the substrate should be "the semiconductor substrate".

Referring to claim **40**, line 13: the phrase "the second metallic " is misdescriptive. The second metallic should be the first metallic.

Appropriate correction is required.

Claims **29-32** are object since each includes the limitation of independent claim 28.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims **36** is rejected under 35 U.S.C. 103(a) as being unpatentable over Clayton (US 4,656,605) in view of Harada et al. (US 5,313,101).

Art Unit: 2811

Clayton teaches a memory module, comprising (Fig.2 & Col.2, lines 49-57):

a substrate comprising a circuit board (Col.2, lines 50-52); a plurality of memory chips (10-18) mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprising a random access memory (RAM) fabricated on a semiconductor substrate; and a connector on the substrate, said connector being wired to said memory circuit. Clayton does not expressly teach that the memory chip comprises a random access memory fabricated on a semiconductor substrate comprising:

a memory circuit region in the semiconductor substrate; a first dielectric over the memory circuit region; a first metallic layer, said first metallic layer comprising aluminum; a contact interconnect between the first metallic layer and the substrate; a second dielectric layer over the first metallic layer; a via hole extending through the second dielectric layer to a surface of the first metallic layer; a titanium aluminide layer lining a bottom of the via hole; a conductive plug material on the titanium aluminide layer, said conductive plug material comprising aluminum; and a second metallic layer on the second dielectric layer and electrically connected to the conductive plug material.

Harada et al. teach a semiconductor integrated circuit device, comprising (Fig.1 & Col.8, line 50 – Col.9, line 11):

a memory circuit region (2) in a semiconductor substrate; a first dielectric (3) over the memory circuit region; a first metallic layer (4), said first metallic layer comprising aluminum (Col.8, lines 58); a contact interconnect between the first metallic layer and the semiconductor substrate; a second dielectric layer (5) over the first metallic layer; a

Art Unit: 2811

via hole extending through the second dielectric layer to a surface of the first metallic layer; a titanium aluminide layer (206) lining a bottom of the via hole; a conductive plug material (103) on the titanium aluminide layer, said conductive plug material comprising aluminum; and a second metallic layer on the second dielectric layer and electrically connected to the conductive plug material. Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the semiconductor integrated device as taught by Harada into the memory module of Clayton since the titanium aluminide intermetallic layer helps to reduce the electron-migration and stress-migration at the via hole.

Allowable Subject Matter

6. Claims **26, 27 & 38** are allowed.
7. Claims **28-35, 37 & 39-40** would be allowable if rewritten or amended to overcome the objection, set forth in this Office action.

The following is an examiner's statement of reasons for allowance and for the indication of allowable subject matter:

Although, Harada teaches a semiconductor integrated structure having a titanium aluminide lining a bottom of the via hole, a titanium layer on sides of said via hole, and a conductive material on the titanium aluminide layer being in contact at an interface, Harada differs from the present claimed invention because, among other things, Harada performs heat treatment to form titanium aluminide after forming conductive material (titanium nitride) on the titanium layer, thereby this tends to create a tensile stress at the interface while the titanium layer reacts with the aluminum, whereas the present claimed

Art Unit: 2811

invention performs heat treatment before forming titanium nitride. In the present claimed invention, the interface is free from tensile stress because the conductive material (titanium nitride) is deposited after heating treatment.

Harada fails to teach or suggest a titanium aluminide lining a bottom and sides of the via hole.

Accordingly, one of ordinary skill in the art would not have been motivated to modify the teaching Harada to further to meet the claimed limitation as set forth in the present claimed invention.

Response to Arguments

8. Applicant's arguments with respect to claim 36 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghee Kang whose telephone number is 703-305-9147. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Application/Control Number: 09/371,955

Page 7

Art Unit: 2811

Donghee Kang

Donghee Kang
Patent Examiner

dhk
January 13, 2003